

## REMARKS

In response to the above-identified Office Action, the Applicant submits the below remarks and respectfully requests reconsideration of the application, as amended, in light of these remarks. The drawings have been amended to overcome the Examiner's objection. No new matter has been added.

The Examiner rejected claims 1-6 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims, as amended, overcome this rejection.

The Examiner rejected claims 1-3 under 35 U.S.C. 102 (e) as being anticipated by U.S. Patent 6,303,448 (hereinafter Chang). The Examiner rejected claims 4-6 under 35 U.S.C. 102 (a) as being anticipated by U.S. Patent 5,918,134 (hereinafter Gardner). The Examiner rejected claims 7-9 under 35 U.S.C. 102 (b) as being anticipated by U.S. Patent 5,342,796 (hereinafter Ahn). The Applicant respectfully traverses these rejections for the reasons set out below.

Applicant contends that references individually or in combination do not teach or suggest all limitations of claim 1, or the other independent and dependent claims of the present application. The Applicant's arguments shall be presented with respect to claim 1. However, these comments are applicable to the other independent and dependent claims of the present application, and the Examiner is respectfully requested to consider these comments and remarks when reviewing the other independent claims for allowability.

With respect to claims 1-3, Chang does not teach or suggest the invention as claimed, specifically Chang does not teach or suggest at least the source/drain terminals comprising an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, an entire innermost side of the extension is adjacent to sidewalls of the recess, a portion of the gate dielectric layer overlaying an innermost portion of the extension. In Change the

source/drain regions 66 are adjacent and superjacent the gate oxide layer 62, thus, the entire innermost portions of the source/drain region 66 is not adjacent to sidewalls of the gate oxide layer as illustrated in Figure 6 of Chang. Thus, Chang does not disclose or suggest the invention, as claimed.

With respect to claims 4-6, Gardner does not teach or suggest the invention as claimed, specifically Gardner does not teach or suggest at least the source/drain terminals comprising an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, an entire innermost side of the extension is adjacent to sidewalls of the recess, a portion of the gate dielectric layer overlaying an inner-most portion of the extension. As illustrated in Figure 10 LDD regions 130 are subjacent a gate dielectric structure 132 and entire innermost portion of the LDD regions 130 is not adjacent to sidewalls of the recess. Thus, Gardner does not teach or suggest the invention, as claimed.

With respect to claims 7-9, Ahn does not teach or suggest the invention, as claimed, specifically, Ahn does not teach or suggest at least a gate electrode completely overlying the gate dielectric layer. The Office Action cites Figure 9 of Ahn as showing all elements of the invention, as claimed, but the element of a gate electrode completely overlying the gate dielectric layer. The Office Action cites Figure 7 of Ahn as showing a gate electrode completely overlying the gate dielectric layer. However, in Figure 9 is a final semiconductor device of Ahn's invention as described in Column 3, lines 61-68. Figure 7 is an intermediary step in forming the final semiconductor of Figure 9. Figure 7 does not illustrate source/drain terminals comprising extensions, which extend to a more shallow depth. Moreover, in Figure 7 the gate electrode 9 does not completely overly a gate oxide film 7 formed on a dug part 16. There is portion of oxide film that surrounds the vertical sidewalls of the electrode 9. In addition, Figure 9 does not illustrates a gate electrode completely overlying the gate dielectric layer either, as implicitly admitted by

the Office Action, when citing Figure 7 rather than Figure 9 as allegedly showing a gate electrode completely overlying the gate dielectric layer. Thus, Ahn does not teach or suggest the invention, as claimed.

The Applicant submits that the rejections under 35 U.S.C. § 112, second paragraph, 35 U.S.C. § 102 (a) and §102 (b) have been addressed, and withdrawal of these rejections is respectfully requested. The Applicant furthermore submits that all pending claims are in condition for allowance, which is earnestly solicited.

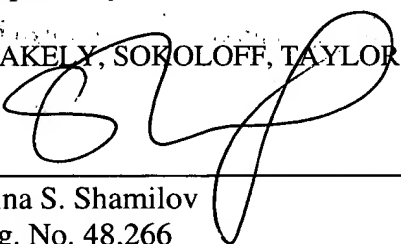
If Examiner Kang believes that a telephone conversation may expedite the prosecution of this case, the Examiner is invited to call Saina S. Shamilov at (408) 720-8300.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicants hereby request such an extension.

Respectfully submitted,

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### **MARKED UP VERSION OF THE CLAIMS**

Please amend the following claims.

1. (Five Times Amended) A field effect transistor, comprising:  
a substrate having a recess in a surface thereof, the recess having a bottom portion and substantially vertical sidewalls;  
a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the substantially vertical sidewalls;  
a gate electrode completely overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls, said gate electrode extending to a less shallow depth within said substrate than a depth at which the source/drain terminals are disposed; wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, an entire innermost side of the extension is adjacent to [an outside surface] sidewalls of the recess, a portion of the gate dielectric layer overlaying an innermost portion of the extension.

2. (Twice Amended ) The transistor of Claim 1, further comprising a portion of the gate electrode that overlies the innermost portion of the [source/drain] extension.

3. (Twice Amended) The transistor of Claim 2, wherein the gate electrode conforms to [the] a recessed channel.

4. (Five Times Amended) A field effect transistor, comprising:  
a substrate having a recess in a surface thereof, the recess having bottom portion and tapered sidewalls, the tapered sidewall surfaces forming an obtuse angle with respect to the bottom portions of the recess;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the tapered sidewalls;

a gate electrode completely overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, an entire innermost side of the extension is adjacent to [an outside surface] sidewalls of the recess, a portion of the gate dielectric layer overlaying an inner-most portion of the extension.

5. (Twice Amended) The transistor of Claim 4, wherein a portion of the gate electrode overlies an innermost portion of the [source/drain] extension.

6. (Amended) The transistor of Claim 4, wherein the gate electrode conforms to [the] a recessed channel.

9. (Twice Amended) The transistor of Claim 7, wherein the gate electrode conforms to [the] a recessed channel.